CMOS DEVICE INTEGRATION FOR LOW EXTERNAL RESISTANCE

ABSTRACT OF THE DISCLOSURE

The present invention relates to a Complementary Metal Oxide Semiconductor (CMOS) device having a lower external resistance and a method for manufacturing the CMOS device. The inventive MOSFET is produced by forming first silicide regions in a substrate as well as atop surface of a gate region and forming second silicide regions where second silicide thickness is greater than the first silicide thickness. The inventive method produces a low resistance first silicide in close proximity to the channel region of the device, where the incorporation of the first silicide decreases the external resistance of the device while the incorporation of the second silicide produces low sheet resistance interconnects.